## R.T.M. Nagpur University
### Scheme of Examination for
#### M. Tech. (VLSI) First Semester

<table>
<thead>
<tr>
<th>Sub. Code</th>
<th>Name of Subject</th>
<th>Teaching Scheme (Clock Hours / Week)</th>
<th>Assessment of Marks of Theory</th>
<th>Assessment of Marks for Practical</th>
<th>Duration of Papers</th>
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<tr>
<td></td>
<td></td>
<td>L</td>
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<td>P/D</td>
<td>Total</td>
</tr>
<tr>
<td>IFU-01</td>
<td>VLSI Subsystem Design</td>
<td>3</td>
<td>-</td>
<td>2</td>
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<td>IFU-02</td>
<td>Modeling Digital System-I</td>
<td>3</td>
<td>-</td>
<td>2</td>
<td>5</td>
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<td>IFU-03</td>
<td>Switching Theory &amp; Automata</td>
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<td>1</td>
<td>-</td>
<td>4</td>
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<td>IFU-04</td>
<td>Advanced Digital Signal Processing</td>
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<td>IFU-05</td>
<td>Embedded System-I</td>
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Total (T+P) = 700

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### Second Semester

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<th>Name of Subject</th>
<th>Teaching Scheme (Clock Hours / Week)</th>
<th>Assessment of Marks of Theory</th>
<th>Assessment of Marks for Practical</th>
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<td>P/D</td>
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<td>IIFU01</td>
<td>Analog VLSI Design</td>
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<td>VLSI Signal Processing</td>
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Total (T+P) = 700
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<th>Sub. Code</th>
<th>Name of Subject</th>
<th>Teaching Scheme (Clock Hours/Week)</th>
<th>Assessment of Marks of Theory</th>
<th>Assessment of Marks for Practical</th>
<th>Duration of Papers</th>
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<tr>
<td>IIFU01</td>
<td>VLSI Testing</td>
<td>3 1 - 4</td>
<td>70 30</td>
<td>100 50</td>
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<td>IIFU02</td>
<td>Elective-II</td>
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<td>200 100</td>
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**Third Semester**

**Elective-I**
1) Advanced Computer Architecture
2) Low Power VLSI Design
3) Embedded System-II

**Elective-II**
1) Mixed Signal Processing
2) Computer Communication Networks
3) Computer Graphics
R.T.M. Nagpur University  
Scheme of Examination for  
M. Tech. (VLSI)  
Fourth Semester

<table>
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<th>Sub. Code</th>
<th>Name of Subject</th>
<th>Teaching Scheme (Clock Hours / Week)</th>
<th>Assessment of Marks of Theory</th>
<th>Assessment of Marks for Practical</th>
<th>Duration of Papers</th>
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<td>P/D</td>
<td>Total</td>
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<td>IVFU01</td>
<td>Thesis / Dissertation (Viva-Voce)</td>
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Note:  
a) Minimum Passing Marks is 50% in all Subjects.  
b) Dissertation Marks will be given based on Internal Seminar & Viva-Voce.
Syllabus for M.Tech.(VLSI)

First Semester Syllabus

IFUV01 VLSI SUBSYSTEM DESIGN

Section A


Section B


Data-Path and Memory Circuits : Static/Dynamic memories, Ancillary memory Analog Circuits.

Books:

IFUV02 MODELLING OF DIGITAL SYSTEM – I

Section A

Programming Technologies – ROMs & EPROMs PLA . PAL gate Arrays Programmable gate arrays and applications, Antifuse FPGA, Synthesis methods for FPGA.


Section B

Chip Level Modeling : Chip level modeling structures modeling delay, process model graphs, Functionally partitioned models, Timing Assertion, Setup & Hold time for clocked devices, Design rule checks

System Modeling : Modeling system interconnection, general model for signal interconnection, Multiplexing of signals. Multiple valued logic. Processor model. RAM model. UART model. Parallel I/O Ports, Interrupt controller Simulation with the physical model, simulation, writing test bench, converting real and interconnection, Multiplexing of signals. Multiple valued logic. Processor model. RAM model. UART model. Parallel I/O Ports, Interrupt controller.

Simulation with the physical model, simulation, writing test bench, converting real and integer to time. Dumping results into text file, reading vectors from text file, test bench example.

Books:

IFUV03 SWITCHING THEORY AND AUTOMATA

Section A

Shannon’s expansion theorem, Consensus theorem, Octal designation, Run measure, INHIBIT/INCLUSION/AOI/Driver/ Buffer gates, gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.
Linear seperability. Unateness, Physical implementation, Dual comparability, Reduced functions, various theorems In threshold logic, Synthesis of single gate and multigate threshold Network. Elementary symmetric functions, partially symmetric and totally symmetric functions, Mc-Cluskey decomposition method. Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.
Mealy Moore State Tables and Systems. State tables from Word Descriptions, Special Methods for Multi Condition Sequence Detectors, Analysis of Finite State Machines.

Section B

Minimization of sequential Machines, State Equivalence and State Table Reduction, machine Equivalence, incompletely Specified machines, Special Heuristic State Table Reduction.
Asynchronous Sequential Machines : Fundamental Mode Systems, pulse Mode Systems, Pulse In, Pulse Out (Mealy), Pulse In, level Signal Out (Moore), Hazards. Structure of and Dependencies in Sequential Machines.
Homing trees and Experiments. Synchronizing Trees and Experiments, Distinguishing Trees and Experiments, Machine Identification, Diagnosable Machines Memory Definiteness and Information Loss less ness.
Memory Span, Input –Output Memory, Output Memory, Input Memory, Information Loss less Machines, Synchronaizable and Uniquely Decipherable Codes.
Finite State Recognizers : Deterministic Recognizers, Transition graphs, Deterministic Graphs from Non deterministic Graphs, Regular Expressions, Regular Sets from Transition graphs.

Books:

IFUV04 ADVANCED DIGITAL SIGNAL PROCESSING

Section A

Multirate Signal processing : Introduction Sampling and signal Reconstruction sampling rate conversion. Decimation by an integer factor, interpolation by an integer factor, Sampling rate conversion by rational factor. Sampling rate converter as a time variant system, practical structures for decimators and interpolators. Direct from and Polyphase FIR structures, with time varying coefficients.
Multirate FIR Filter Design. Design of FIR filters for sampling rate conversion. Multistage implementation of sampling rate conversion, Applications of Interpolation and decimation in signal processing operations low pass and band pass filters, filter bank implementation, sub band processing, Decimated filter banks. Two channel filter banks, QMF filter banks, perfect reconstruction filter banks tree structure filter banks octave, band filter banks, uniform DFT filter banks.

Section B

methods, Sequential estimation, Moving average and ARMA models, minimum variance method, Pizarenko’s harmonic Decomposition method, MUSIC method.

Books:
1. Oppenhiem and Sohaffer, “Discrete time signal processing”, Prentice hall

IFUV05          EMBEDDED SYSTEM – I

Section A

The 8051 micro controller, Assembly language programming Jump, Loop and Call instructions, I/O port programming, Addressing modes, Arithmetic Instructions and programs Logic Instructions and programs, Single bit Instructions.

Section B

Timers and counters Serial Communications, Interrupts programming Interfacing LCD, ADC and sensors, Interfacing stepper motors, keyboards and DAC’S. Interfacing external memory and 8255

Books:

Second Semester M. Tech (VLSI) Full Time

IIFUV01          ANALOG VLSI DESIGN

Section A

Device modeling and simulation Modeling, MOS Models Diode model, Bipolar modes BSIM Spice models, Circuit simulations using Spice.

Section B

Analog signal processing, CMOS Digital to analog converters, Scaling and serial, cyclic. Analog to digital converters Serial, SAR, Parallel, Pipelined, sigma-delta converters, mixed signal Layout issues.
Continuous time filters, Switched capacitor filters, Modulator and multipliers, PLL.

Books:

IIFUV02          MODELLING OF DIGITAL SYSTEM-II
Section A

Introduction to Verilog, Module, delays, descriptions, Language elements, Expressions, Gate-level modeling User defined primitives, Dataflow modeling, Behaviour modeling, Structural modeling, Tasks and functions.
Programmable Logic Devices: Basis concept, Programming technologies, Programmable logic elements, programmable logic array, programmable array logic, structure of standard PLD’s, complex PLDs CPLD. Altera Max 7000 series. AMD Match 4 structure.

Section B

System Design with PLD’S : Design of combinational and sequential circuits using PLD’s, Programming PAL devices, using PALASM, Design of state machines using algorithmic state machines ASM chart as a design tool
Introduction to FPGA: types of FPGA, Xilinx XC3000 series, Logic Cell Array (LCA), Configurable Logic Blocks (CLB), Input/Output Blocks (I/OB), Programmable interconnection Points (PIP), introduction to ACT 2 family and Xilinx4000 families, Design example.

Books:

VLSI SIGNAL PROCESSING

Section A

Pipelining and Parallel Processing: introduction, pipeling of FIR Digital filters Parallel processing. Pipelining and parallel processing for low power.
Retiming: Introduction, Definition and properties, Solving system of inequalities, retiming techniques.
Unfolding Introduction An algorithmsfor unfolding, Properties of unfolding, Critical path, unfolding and retiming Application of unfolding.
Folding: Introduction Folding Transformation, Register Minimization Techniques, Register minimization in folded architectures Folding if Multirate systems.

Section B

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR systolic Arrays, Selection of scheduling vector, Matrix Multiplication and 2D systolic array Design, Systolic design for space representations containing Delays.
Fast Convolution: Introduction, Cook, Toom algorithm, Winogard algorithm, iterated convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

Books:
DIGITAL IMAGE PROCESSING

Section A


Image Transforms: Need for image transform Walsh transform hotel ling transform.


Section B


Books:
1. Rafael C. Gonzalez and Richard E. Woods “Digital image processing”, Addition-wisely
1. Huang T.S. “Picture processing and digital filtering” Springer Verlag Berlin Heidelberg.

ELECTIVE –I

ADVANCED COMPUTER ARCHITECTURE

Section A


Section B

Parallel and scalable architectures Multiprocessor and Multi computers, Multi vector and SIMD computers, Scalable, Multithreaded and data flow architectures.

Parallel models, Languages and compilers, Parallel program development and environments, IM INIX MACH and OSF/1 for parallel computers.

Books:
3) M.J. Quinn, “Designing Efficient Algorithms for Parallel Computers”
IIFUV05(B)  LOW POWER VLSI DESIGN

Section A


Section B


Books:

IIFUV05 (C)  EMBEDDED SYSTEM – II

Section A


Section B

OS services. Operating Modes. Threads, Context Switching overheads, Scalability, Embedding with application code. Task Scheduling. Interrupt handling. Inter task communication. Comparison and application of various RTOS.

Books:
3) Jean J. Labrosse, “Micro C/OS II The Real Time Kernel”
4) Richard H. Barnett, Sarah A Cox Larry D, “Embedded C Programming and Atmel AVR”

Syllabus of Examination for
Third Semester M. Tech (VLSI) Full Time

IIFUV01  VLSI TESTING

Section A

Exponential nature of the testing problem, Fault models, Stuck-at-faults, Test generation for combinational circuits, The D algorithm. POCEM, FAN, Learning Algorithms, Fault converge, Fault simulation and fault grading, Testability measures, Test generation, algorithms for sequential circuits, Scan and practical scan design, BIST and other design for testability techniques.

Section B

Boundary scan and the IFEE 11491 testability standard CMOS opens testing, performance and delay testing, IDDQ and other current based tests.
Synthesis for testability, Memory testing, Mixed signal testing.
Test. Effectiveness: coverage, yield and defect level, System-level test and diagnosis, MCM and core based testing.

Books:

IIIFUV02 ELECTIVE – II

IIIFUV02(A) MIXED SIGNAL PROCESSING

II. Section A

Analog and Mixed Signal Extensions To VHDL: Introduction, language design objectives, theory of differential algebraic equation the 1076.1. language tolerance groups, conservative system, time and simulation cycle A/D and D/A interaction, quiescent point, frequency domain modeling and examples.

Section B

Analog Extensions To Verilog: Introduction Equation construction solution, waveform filter functions, simulator, control analysis, multi-disciplinary model.
Non-Linear state space averaged modeling of 3-state – digital phase-frequency detector.
Introduction model, resell table integrator AC analysis, sample application.

Books:

IIIFUV02 (A) COMPUTER COMMUNICATION NETWORKS

Section A

Introduction: Goals uses Network components, switching technologies network topologies transmission media, protocol, routing and flow, WAN, MAN, LAN, ARPANET.
Queueing Theory: Importance Queueing modes, Poisson statistics, little theorem, M/M/I and models, applications to computer networks.
Comparison, applications, implementation procedure MAN and its IEEE standards switched and fast Ethernet. FDDI, and SONET.

Section B
Network protocols: Concept, functions, goals of layered Architecture, OSI reference model, X-25, Frame relaying. TCP/IP architecture and operations. The IP layers and function naming addressing and routing in an internet, major application layers user services: E-mail, WEB, HTTP, TEONET.


Broadband networks: Telecommunication networks, evolution ISDN: structures limitation –ISDN(B) services transfer modes asynchronous transfer mode(ATM) characteristics, protocols reference model, ATM cell format, ATM services and quality of services, classes of traffic and traffic management concept, introduction to VAST networks.

Books:


IIIFUV02(C) COMPUTER GRAPHICS

Section A

Introduction to computer graphics, Raster refresh graphics displays, cathode ray tube basics, color CRT Raster Scan Basics, video-basics.

Line drawing algorithms, Bresharm’s algorithms, DDA, Bresharm’s Circle generation algorithm. Run length encoding cell coding Real time scan conversion Quad Trees.

Section B

Polygon filling methods grouping techniques for lines polygons, Three dimensional transformation. Hidden lines & surface Rendering, Curve generation, Brnzier and B-spine curves.

Architecture of VGA, ROMBIOS. Text operation. Graphics Modes controller, introduction to GKS Practical will be based on C++& Windows.

Books: